REMARKS/ARGUMENTS

This amendment is responsive to the office action mailed on February 17, 2004.

Claims 1-31 are pending in this application. No claims are canceled. Claims 1, 4, 8, 11, 14, 18 and 21 were amended to more distinctly claim the invention. Claims 8 and 18 were also amended so that they are in independent form. New claims 25-31 have been added to more distinctly claim the invention. Support for the amendments and the new claims are found in the specification, and no new matter has been added.

35 U.S.C. §103 Rejection, Alwais et al. in view of Leung et al..

Claims 1-24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent no. 5,991,851 to Alwais et al. (Alwais) in view of U.S. patent no. 5,394,534 to Leung et al. (Leung). Reconsideration and allowance of claims are respectfully requested for the following reasons.

Claim 1 recites a memory device, "wherein logically adjacent rows are placed in different sub-arrays, wherein a first row is in a first sub-array and a second row is in a second sub-array, the second row being one logical row from the first row, and a third row is in the first sub-array and a fourth row is in the second sub-array, the fourth row being one logical row from the third row." Alwais does not have this feature of the invention.

More specifically in figure 3, Alwais does not show or suggest placing two sets of two logically adjacent rows into two sub-arrays. By allocating logical rows in the fashion recited in claim 1, the present invention reduces the possibility that any one sub-array will become too far behind in its refreshes. See page 9, lines 9-10. Alwais does not have this feature of the invention.

Accordingly, claim 1 and its dependent claims are allowable.

Claim 4 recites that "the non-array row comprises at most one SRAM row." Leung does not show or suggest the non-array row comprising at most one SRAM row, but only describes an SRAM cache with a sufficient number of rows.

More specifically in figure 1, Leung refers to an SRAM cache (187). In col. 5, lines 51-52, Leung states that the SRAM cache (187) has the same organization as the DRAM banks. The summary of the invention states "[t]he S[R]AM cache is selected to have a capacity sufficient to ensure that each of the memory banks is refreshed properly within a predetermined refresh period . . . even under the worst cache-thrashing conditions." See col. 2, lines 59-63. This means that the SRAM must be large enough to ensure that "one cache hit or memory idle cycle will occur . . . during each refresh timer period." See col. 10, lines 54-56.

In Leung, if the cache was at most one SRAM row, the cache would not be large enough to ensure that a cache hit or memory idle cycle would occur under the worst cache-thrashing conditions. This would cause a delay in external access to memory. This delay would be the reverse of Leung's express purpose of the invention: "The control circuit controls the accessing and refreshing of the memory cells such that the refreshing of the memory cells does not interfere with any external access of the memory cells." See col. 2, lines 30-33. Leung does not allow for handling such an interference or delay, thus Leung's invention would not work under such conditions. Finally, the DRAM banks are required to be of a sufficient number of rows to provide the memory density desired for Leung's invention. See col.1, lines 22-26.

In this invention, the "serial refresh operation" (page 8, line 15) allows having the non-array row be at most SRAM row because while a sub-array row is being accessed, a non-accessed row in the same sub-array can be refreshed. Alwais does not teach or suggest this feature of the invention.

Accordingly, claim 4 is allowable.

Claim 8 recites refresh circuitry, "wherein the refresh circuitry further comprises a refresh timer for setting a minimum time between refresh cycles." In contrast, Alwais describes a method for enforcing a maximum time since a row was last refreshed.

In figure 6, Alwais describes a refresh process. This refresh process begins with a test to see if the memory device is active. See col. 9, lines 4-6. If the memory device is active, then a refresh delay counter is incremented. Subsequently, the value of the delay counter is checked to see if it is a certain maximum value (e.g., 128). If so, a refresh is done regardless of whether the memory device is active. See col. 9, lines 14-21. This step ensures that the maximum allowed time since a row was last refreshed is not exceeded, so no information is lost.

In contrast, in the present invention, the refresh timer is for setting a minimum time between refresh cycles performed. At page 5, lines 4-20, the detailed description explains how this step ensures that power is not adversely wasted by running refreshes excessively often. Alwais does not teach or suggest this feature of the invention.

Accordingly, claim 8 and its dependent claims are allowable.

Claim 11 recites similar features as recited for claim 1, and claim 11 and its dependent claims should be allowable for at least similar reasons as claim 1.

Claim 14 recites similar features as recited for claim 4, and claim 14 should be allowable for at least similar reasons as claim 4.

Claim 18 recites similar features as recited for claim 8, and claim 18 and its dependent claims should be allowable for at least similar reasons as claim 8.

Claim 21 recites a memory device comprising "a comparator for internally determining when a refresh cycle can be hidden behind an access to the non-array row."

Alwais does not teach or suggest this feature. At col. 4, lines 22-39, Alwais gives a more detailed illustration of a "memory" decoder (Fig. 1, Ref. 18) as having a row comparator (66) in figure 2. The comparator determines if the requested memory is in the SRAM cache (col. 4, lines 31-45), not to determine when a refresh cycle can be hidden behind an access to the non-array row. In col. 9, lines 1-3, Alwais uses the word "hidden" in referring to refreshes done via the process of figure 6, which delays refreshes. Nowhere does Alwais mention hiding a refresh

cycle "behind an access to the non-array row." Thus, claim 21 and its dependent claims are allowable for at least this reason.

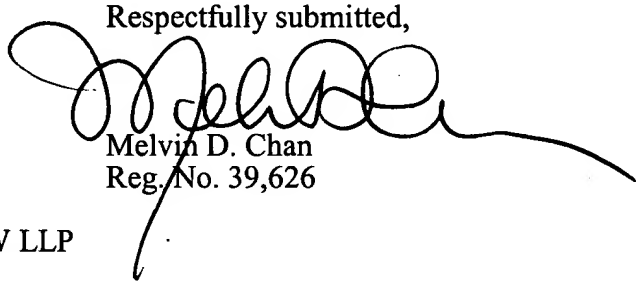
Furthermore, claim 21 also recites a memory device comprising "a controller for setting a minimum time between refresh cycles to a subset of possible times internally determined by the comparator." This imitation is similar to that discussed for claim 8 above, and therefore claim 21 and its dependent claims should be allowable for at least this additional reason.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



Melvin D. Chan
Reg. No. 39,626

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 415-576-0300
Attachments
MDC:dbr
60247105 v1